A 110MHz 84dB CMOS Programmable Gain Amplifier with RSSI

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Abstract — **This paper describes a CMOS programmable gain amplifier that maintains a 3dB bandwidth greater than 110MHz and can provide 84dB gain control range in 1dB steps. The PGA can also be operated in a low power mode with 3dB bandwidth greater than 71MHz. Integrated with this PGA is a CMOS successive logarithmic detecting amplifier with a ±0.7dB logarithmic accuracy over 80dB dynamic range. It achieves a sensitivity of -83dBm. The amplifier consumes 13mA from a single 3V supply in high power mode. The chip area including pads occupies 1.5x 1.5mm^2.**

I. Introduction

Although recently zero-IF and low-IF architecture have been widely used recently in wireless telephone handsets to reduce the external component count, super-heterodyne architecture as shown in Fig.1 continues to be widely used due to its overall better performance. Signal processing such as amplifying or filtering are usually realized at the IF frequency in a super-heterodyne system. The circuits will consume less power if the signal processing is performed at IF frequency rather than at RF frequency. Also, offset and flicker noise can be ignored if most of the system gain is realized at IF frequency rather than at baseband.

In wireless communication systems, the received signal exhibits a wide dynamic range after passing through unpredictable propagation channels, so a PGA is typically employed in the signal chain to handle these unpredictable received signals. In the design of a PGA with non-uniform gain distribution such as proposed in reference [1], it is difficult to accompany the circuit with a RSSI function, so the measurement of the received signal strength needs to be performed, for example, at baseband. The tracking speed for the automatic gain control loop will be lowered. In the design of a PGA with uniform gain distribution as proposed in reference [2], the RSSI circuit can be easily added to the PGA circuit, but unfortunately, the RSSI characteristics will change when the gain of the PGA is adjusted, so a mapping from the RSSI output to true signal level is required.

The voltage gain of the proposed PGA in this paper can be programmed from 0dB to 84dB in 1dB steps, which corresponds to a programmable range from -6dB to 78dB in power gain with an input impedance 50Ω and an output impedance 200Ω. With this PGA we also design a received signal strength indicator (RSSI) circuit in order to monitor the signal strength at IF frequency and use it as a reference of how to adjust the gain of the system. The RSSI curve will not change when we vary the gain of the PGA. The PGA circuit we propose can be used in either the received path or the transmit path as shown in Fig.1. In section 2 we will describe the circuit architecture of the proposed PGA with RSSI. The circuit design of the fixed gain amplifier and the fine gain step amplifier is expounded in section 3 and 4, respectively. Section 5 describes the RSSI circuit and some other considerations. The experimental results are shown in section 6. Finally, a simple conclusion is drawn in section 7.

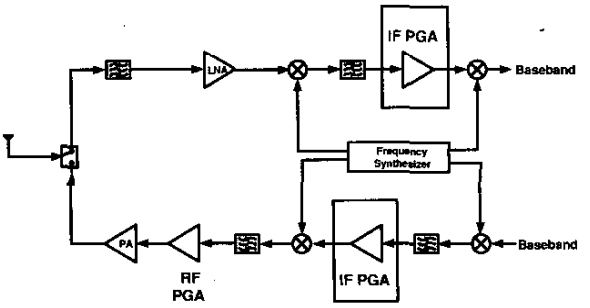

Fig.1 Block diagram of a typical super-heterodyne system

II. The Circuit Architecture

In our design as shown in Fig.2, we also accompany the PGA with a received signal strength indicator circuit, and furthermore, the RSSI curve will not change when we adjust the gain of the whole PGA. The PGA circuit is composed of six fixed gain stages, and each gain stage has 12dB gain. With these six fixed gain stages, we can adjust our gain in 12dB gain step over 72dB range by selecting the input of the PGA or one of the outputs of the six fixed gain stages as shown in Fig.2. We can further increase the resolution of the PGA by passing the selected output signal through a PGA with fine gain steps, for instance 1dB in our design, to cover 12dB range. So the overall gain of the PGA is programmable from 0dB to 84dB in 1dB steps.

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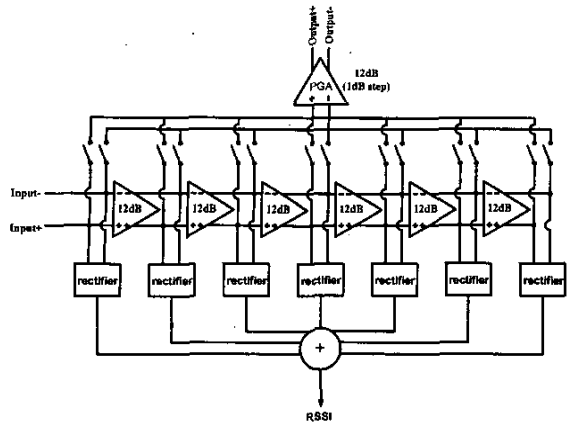

Fig.2 Block diagram of the proposed PGA

III. Fixed Gain Amplifier Design

Due to process variations, the gain of the fixed gain amplifiers may vary from 6dB to 15dB, and this will significantly affect the accuracy of the gain setting of the PGA. To accommodate the gain variation caused by such process variations, we design a gain control bias circuit to generate the bias current for our fixed gain amplifiers, as shown in Fig.3. The circuit compares the gain of the fixed gain amplifier with the gain we set, which is equal to $(R_1+2R_2)/R_1$, and generates the correct bias current to bias the fixed gain amplifiers.

For the fixed gain amplifier we designed, power can be saved by lowering the bandwidth of the amplifier circuit as shown in Fig.3. The load of the fixed gain amplifiers is composed of a resistor in parallel with a voltage controlled resistor (VCR). The gain of the fixed gain amplifier can be obtained as,

$$Av \cong g_{m input} \times R_{RES} \cdot 2\sqrt{K\frac{I_{tail}}{2}} \times R_{RES}$$

$$when \quad R_{RES} \ll R_{VCR} \cdots\cdots\cdots\cdots (1a)$$

$$Av = g_{m input} \times (R_{RES} // R_{VCR}) \quad g_{m input} \quad (R_{RES} // \frac{2}{\lambda I_{tail}})$$

$$when \quad R_{RES} \cong R_{VCR} \cdots\cdots\cdots\cdots (1b)$$

$$Av \cong g_{m input} \times R_{VCR} \quad 2\sqrt{K\frac{I_{tail}}{2}} \quad \frac{2}{\lambda I_{tail}} \cdot 2\sqrt{K}\frac{\sqrt{2}}{\sqrt{I_{tail}}}$$

$$when \quad R_{RES} \gg R_{VCR} \cdots\cdots\cdots\cdots (1c)$$

where $K=(1/2)\,\mu_n C_{OX}(W/L)$ and λ is the channel length modulation coefficient. In order to find out the maximum gain of the fixed gain amplifier, we can take the differentiation of (1b) with respect to I_{tail} and it will be shown that the maximum gain occurs when the resistance of the VCR is equal to the resistance of the resistor. This means the maximum gain is achieved when the tail current is $2/(\lambda \times R_{RES})$. When the resistance R_{RES} of the resistor is much lower than the resistance R_{VCR} of the VCR, the load resistance is dominated by R_{RES}. So the gain of the fixed gain amplifiers can be enlarged by increasing the tail current as shown in (1a). And the 3dB bandwidth of the amplifier is determined by the pole $1/(2\pi \times R_{RES} \times C_{output})$ formed by the load resistance, i.e. R_{RES}, and the capacitance C_{output} at the output node. When R_{VCR} dominates the resistance of load, i.e. R_{VCR} is much smaller than R_{RES}, the gain of the fixed gain amplifier can be enlarged by decreasing the tail current of the amplifier as shown in (1c). And under the circumstance that R_{VCR} is much smaller than R_{RES}, the 3dB bandwidth of the fixed gain amplifier is approximately $1/(2\pi \times R_{VCR} \times C_{output})$. Since R_{VCR} is smaller than R_{RES} which is a fixed value, we can expect that the 3dB bandwidth is larger when the R_{VCR} dominates the load resistance and meanwhile the power consumption is also higher. As long as the IF frequency does not exceed the bandwidth of the PGA in low power mode, power can be saved by operating the circuit in the low power mode.

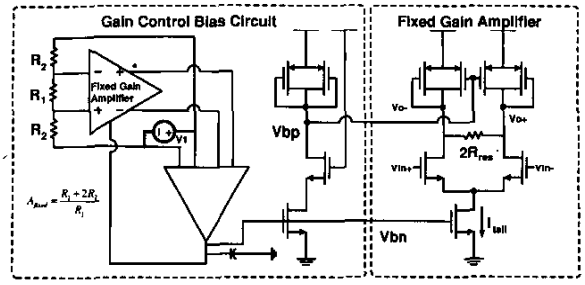

Fig.3 Fixed gain stage and gain control bias circuit

IV. Fine Gain Step Amplifier Design

In order to achieve fine gain step adjustment, one fine gain step PGA with 1dB steps over 12dB range is arranged at the end of the signal chain. The circuit of this PGA is shown in Fig.4. The gain step is determined by the ratio of the gain control transistor M3 to M4 and M5 to M6. The gain of the PGA can be expressed as the following equation:

$$A_{PGA-1dB} = g_{m1,2} \quad \frac{K_3 - K_4}{K_3 + K_4} \quad r_o \qquad (2)$$

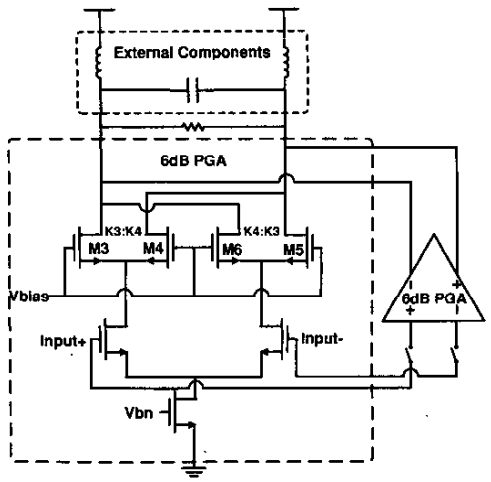

Fig.4 Fine gain step PGA amplifier

The ratio of K_3 to K_4 chosen for the voltage gain setting of the fine gain amplifier from 0dB to 6dB with respect to the minimum gain is listed in Table I. For example, the gain set by choosing K_3:K_4=18:5 is 1dB larger than the gain set by choosing K_3:K_4=18:6. For voltage gain from 7dB to 12dB, we simply apply another 6dB PGA in

TABLE I
SUMMARY OF VOLTAGE GAIN SETTINGS

Gain Setting	K_3:K_4	Gain Setting	K_3:K_4
0dB	18:6	4dB	18:2
1dB	18:5	5dB	18:1
2dB	18:4	6dB	18:0
3dB	18:3		

parallel with the former 6dB PGA. These are shown in Fig.4. The change of the total width of gain control transistors M3 and M4 (M5 and M6) should be as small as possible so that the variation of the voltage at point X (point Y) won't significantly influence the g_m of the input transistors M1 and M2. If the variation of the voltage at point X (point Y) is too large, the gain step error will also increase due to the significant influence on the g_m of the input transistors M1 and M2. The differential output points are connected to the power supply through two external inductors that can improve the linearity of the PGA. These two inductors together with the capacitor between the differential output nodes also provide bandpass filtering and impedance matching functions.

V. RSSI CIRCUIT AND OTHER DESIGN CONSIDERATIONS

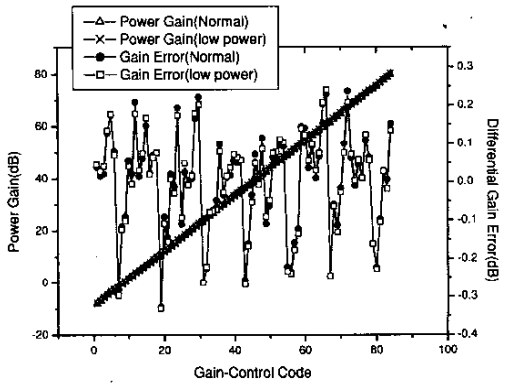

Fig.5 IF amplifier power gain and gain error

The RSSI circuit is the same as that proposed in reference [3], and it can function well in spite of the process variations. The coarse gain step adjust circuit must be designed carefully to eliminate the reverse signal coupling from the output of the last stage of the fixed gain amplifier chain, otherwise the circuit may oscillate. Double guard rings are used to prevent substrate coupling. The first fixed gain stage must also be carefully designed because the offset cancellation circuit will deduce the gain of the first stage. We have designed the first fixed gain stage with a little higher gain to compensate the loss.

VI. EXPERIMENTAL RESULTS

The IF amplifier we proposed has been fabricated in a 0.35 μm 1P4M CMOS process. The capacitors used for frequency compensation in our operational amplifier for the bias circuit are realized using MOS capacitors. The gain programming logic circuit and RSSI circuit are also integrated with this IF amplifier. The test chip is directly bonded to a PCB surrounded with the required external components. The programmable power gain range is from -7.78dB to 79.79dB in normal operation (at 110MHz) mode and -7.79dB to 80.03dB ig low power operation (at 71MHz) mode as shown in Fig.5. It can be found that the peaks of gain step error occur every 12 dB because of the 12dB gain of the fixed gain amplifiers. The gain step error is kept within ±0.4dB when the test chip is operated in either mode. The input impedance is 50Ω and the output impedance is 200Ω. In Fig.6 it is shown that the measured RSSI accuracy is ±0.7dB with the input signal varied from -83dBm to -3dBm. The accuracy of the multimeter used for measuring the RSSI circuit is 10mV, which corresponds to about 0.6dB. The measured oCP is

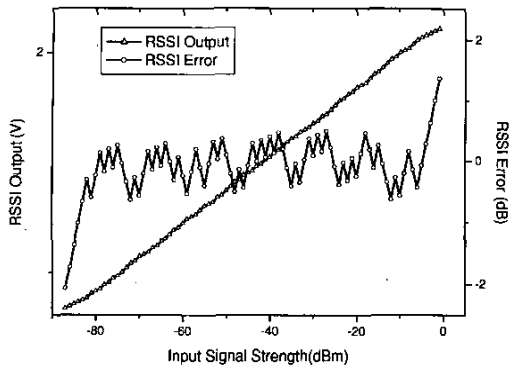

Fig.6 RSSI Output and RSSI Error

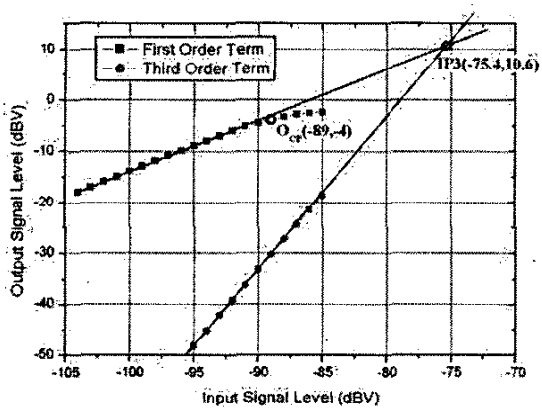

Fig.7 IF Amplifier OCP and IP3

-4dBV and the oIP3 is 10.6dBV which are shown in Fig.7. The IC consumes 13mA from 3V when operated in normal mode and 5mA from 3V when operated in low power mode. The chip micrograph is shown in Fig.8. The chip area including pads occupies $1.5 \times 1.5mm^2$. Table II summarizes the key measured performances.

VI. CONCLUSIONS

In this paper we realized a 110MHz 84dB programmable gain amplifier using standard CMOS technology. Despite of the process variations, the performance can be maintained excellent by using the gain controlled bias circuit. The programmable gain amplifier can be operated when the minimal input signal is -83dBm. High gain step accuracy (±0.4dB) with 1dB resolution is be saved under low power mode when the frequency of the input signal is lower than 74MHz.

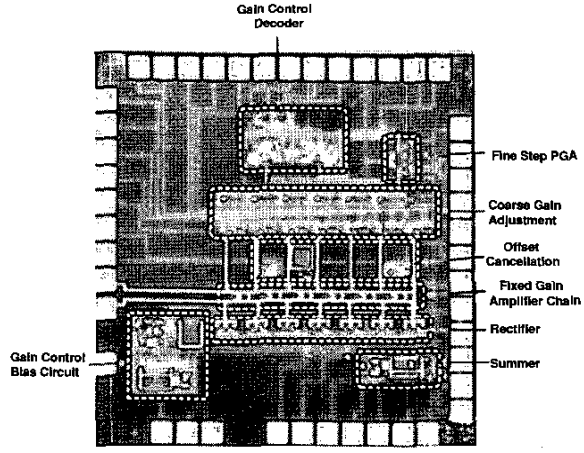

Fig.8 Chip micrograph

TABLE II
SUMMARY OF CHIP PERFORMANCE

Process	0.35 μm CMOS 1P4M
Chip size	$1.5 \times 1.5mm^2$
Maximum gain	79.79dB(high power) 80.03dB(low power)
Minimum gain	-7.78dB(high power) -7.79dB(low power)
Gain step	1dB
Gain step error	-0.4 to 0.3dB
Input impedance	50Ω
Output impedance	200Ω
Supply Voltage	3.0±0.3V
Current consumption	13mA(high power) 5mA (low power)
RSSI accuracy	±0.7dB

ACKNOWLEDGEMENT

The authors would like to thank National Chip Implementation Center and MediaTek Incorporation, Taiwan, for chip implementation and support of this work.

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